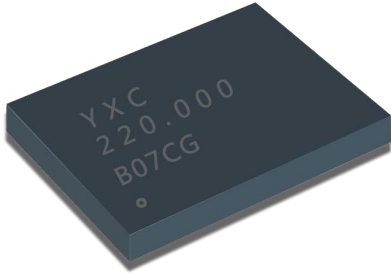




YSO9122MR



Features

- Any frequency between 220 MHz and 625 MHz accurate to 6 decimal places
- LVPECL and LVDS output signaling types
- 0.6ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ± 10 ppm
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 3.2x2.5, 5.0x3.2 and 7.0x5.0 mmxmm
- For frequencies lower than 220 MHz, refer to YSO9121MR datasheet

Applications

- 10GB Ethernet, SONET, SATA, SAS, Fibre Channel, PCI-Express
- Telecom, networking, instrumentation, storage, servers

Electrical Characteristics

| Parameter and Conditions | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-----------------------------------------------------------|-----------|---------|------|---------|------------|--------------------------------------------------------------------------------------------------------|
| LVPECL and LVDS, Common Electrical Characteristics | | | | | | |
| Supply Voltage | Vdd | 2.97 | 3.3 | 3.63 | V | |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 2.25 | – | 3.63 | V | Termination schemes in Figures 1 and 2 - XX ordering code |
| Output Frequency Range | f | 220 | – | 625 | MHz | |
| Frequency Stability | F_stab | -10 | – | +10 | ppm | Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations |
| | | -20 | – | +20 | ppm | |
| | | -25 | – | +25 | ppm | |
| | | -50 | – | +50 | ppm | |
| First Year Aging | F_aging1 | -2 | – | +2 | ppm | 25°C |
| 10-year Aging | F_aging10 | -5 | – | +5 | ppm | 25°C |
| Operating Temperature Range | T_use | -40 | – | +85 | °C | Industrial |
| | | -20 | – | +70 | °C | Extended Commercial |
| Input Voltage High | VIH | 70% | – | – | Vdd | Pin 1, OE or ST |
| Input Voltage Low | VIL | – | – | 30% | Vdd | Pin 1, OE or ST |
| Input Pull-up Impedance | Z_in | – | 100 | 250 | k Ω | Pin 1, OE logic high or logic low, or ST logic high |
| | | 2 | – | – | M Ω | Pin 1, ST logic low |
| Start-up Time | T_start | – | 6 | 10 | ms | Measured from the time Vdd reaches its rated minimum value. |
| Resume Time | T_resume | – | 6 | 10 | ms | In Standby mode, measured from the time ST pin crosses 50% threshold. |
| Duty Cycle | DC | 45 | – | 55 | % | |
| LVPECL, DC and AC Characteristics | | | | | | |
| Current Consumption | Idd | – | 61 | 69 | mA | Excluding Load Termination Current, Vdd = 3.3V or 2.5V |
| OE Disable Supply Current | I_OE | – | – | 35 | mA | OE = Low |
| Output Disable Leakage Current | I_leak | – | – | 1 | μ A | OE = Low |
| Standby Current | I_std | – | – | 100 | μ A | ST = Low, for all Vdds |
| Maximum Output Current | I_driver | – | – | 30 | mA | Maximum average current drawn from OUT+ or OUT- |
| Output High Voltage | VOH | Vdd-1.1 | – | Vdd-0.7 | V | See Figure 1(a) |
| Output Low Voltage | VOL | Vdd-1.9 | – | Vdd-1.5 | V | See Figure 1(a) |
| Output Differential Voltage Swing | V_Swing | 1.2 | 1.6 | 2.0 | V | See Figure 1(b) |
| Rise/Fall Time | Tr, Tf | – | 300 | 500 | ps | 20% to 80%, see Figure 1(a) |
| OE Enable/Disable Time | T_oe | – | – | 115 | ns | f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period |
| RMS Period Jitter | T_jitt | – | 1.2 | 1.7 | ps | f = 266 MHz, VDD = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 312.5 MHz, VDD = 3.3V or 2.5V |
| | | – | 1.2 | 1.7 | ps | f = 622.08 MHz, VDD = 3.3V or 2.5V |
| RMS Phase Jitter (random) | T_phj | – | 0.6 | 0.85 | ps | f = 312.5 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds |
| LVDS, DC and AC Characteristics | | | | | | |
| Current Consumption | Idd | – | 47 | 55 | mA | Excluding Load Termination Current, Vdd = 3.3V or 2.5V |
| OE Disable Supply Current | I_OE | – | – | 35 | mA | OE = Low |
| Differential Output Voltage | VOD | 250 | 350 | 450 | mV | See Figure 2 |

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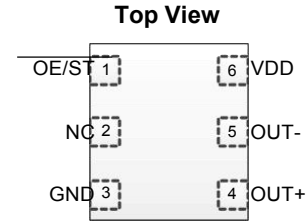


Electrical Characteristics (continued)

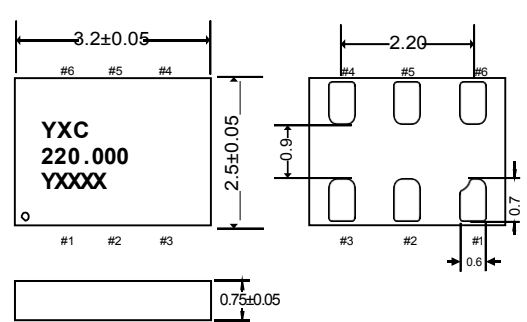
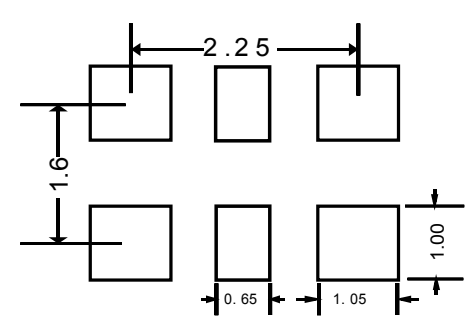
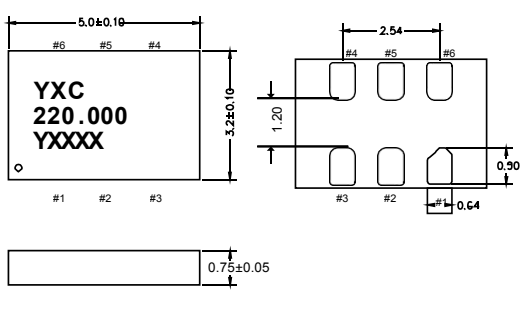
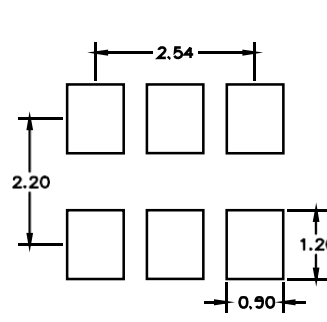
| Parameter and Conditions | Symbol | Min. | Typ. | Max. | Unit | Condition |
|----------------------------------------------------|---------------------------------|-------|------|-------|------|-------------------------------------------------------------------------|
| LVDS, DC and AC Characteristics (continued) | | | | | | |
| Output Disable Leakage Current | I _{leak} | - | - | 1 | μA | OE = Low |
| Standby Current | I _{std} | - | - | 100 | μA | ST = Low, for all Vdds |
| VOD Magnitude Change | ΔVOD | - | - | 50 | mV | See Figure 2 |
| Offset Voltage | VOS | 1.125 | 1.2 | 1.375 | V | See Figure 2 |
| VOS Magnitude Change | ΔVOS | - | - | 50 | mV | See Figure 2 |
| Rise/Fall Time | T _r , T _f | - | 495 | 600 | ps | 20% to 80%, see Figure 2 |
| OE Enable/Disable Time | T _{oe} | - | - | 115 | ns | f = 220 MHz - For other frequencies, T _{oe} = 100ns + 3 period |
| RMS Period Jitter | T _{jitt} | - | 1.4 | 1.7 | ps | f = 266 MHz, VDD = 3.3V or 2.5V |
| | | - | 1.4 | 1.7 | ps | f = 312.5 MHz, VDD = 3.3V or 2.5V |
| | | - | 1.2 | 1.7 | ps | f = 622.08 MHz, VDD = 3.3V or 2.5V |
| RMS Phase Jitter (random) | T _{phj} | - | 0.6 | 0.85 | ps | f = 312.5 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds |

Pin Description

| Pin | Map | Functionality |
|-----|------|------------------------------------------------------------------------------------------------------------------------------|
| 1 | OE | Input H or Open: specified frequency output L: output is high impedance |
| | ST | Input H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I _{std} . |
| 2 | NC | NA No Connect; Leave it floating or connect to GND for better heat dissipation |
| 3 | GND | Power VDD Power Supply Ground |
| 4 | OUT+ | Output Oscillator output |
| 5 | OUT- | Output Complementary oscillator output |
| 6 | VDD | Power Power supply voltage |



Dimensions and Patterns

| Package Size – Dimensions (Unit: mm) ^[1] | Recommended Land Pattern (Unit: mm) ^[2] |
|-------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 3.2 x 2.5x 0.75 mm  |  |
| 5.0 x 3.2 x 0.75 mm  |  |

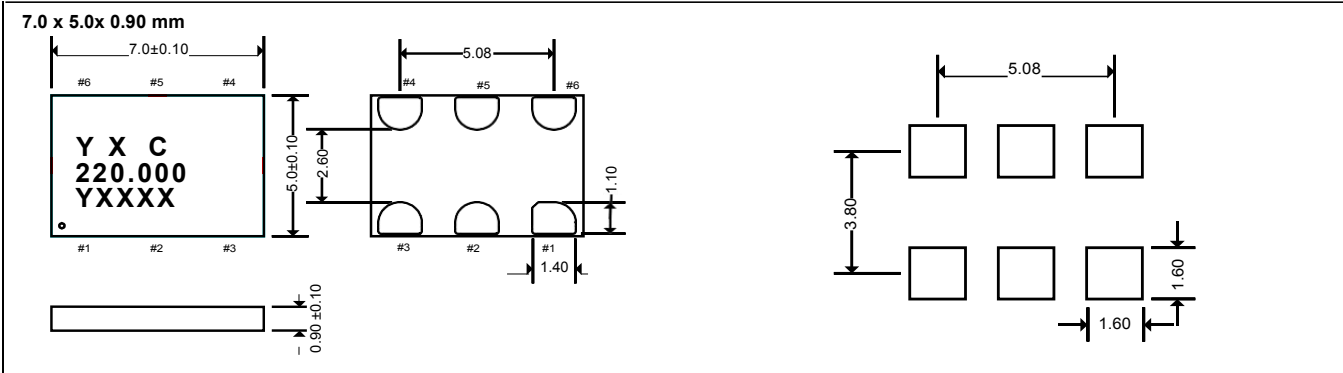


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YSO9122MR



Dimensions and Patterns



Notes:

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
2. A capacitor of value 0.1 μ F between Vdd and GND is recommended.

PART Number Guide

| Quartz Crystal Oscillator | Dimensions | Frequency (Hz) | Supply voltage (V) | Frequency Stability Overall (ppm) | Output | Pin | Material | Operating Temp. Range |
|---------------------------|------------|----------------|--------------------|-----------------------------------|--------|-----|----------|-----------------------|
| O | 7050 | 500M | E | E | B | 6 | M | I |

Frequencies Not Supported

| |
|------------------------------------------------|
| Range 1: From 251.000001 MHz to 263.999999 MHz |
| Range 2: From 314.000001 MHz to 422.999999 MHz |
| Range 3: From 502.000001 MHz to 527.999999 MHz |

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Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|----------------------------------------------------------------------|------|------|------|
| Storage Temperature | -65 | 150 | °C |
| VDD | -0.5 | 4 | V |
| Electrostatic Discharge (HBM) | - | 2000 | V |
| Soldering Temperature (follow standard Pb free soldering guidelines) | - | 260 | °C |

Thermal Consideration

| Package | θ_{JA} , 4 Layer Board (°C/W) | θ_{JC} , Bottom (°C/W) |
|-------------|--------------------------------------|-------------------------------|
| 7050, 6-pin | 142 | 27 |
| 5032, 6-pin | 97 | 20 |
| 3225, 6-pin | 109 | 20 |

Environmental Compliance

| Parameter | Condition/Test Method |
|----------------------------|---------------------------|
| Mechanical Shock | MIL-STD-883F, Method 2002 |
| Mechanical Vibration | MIL-STD-883F, Method 2007 |
| Temperature Cycle | JESD22, Method A104 |
| Solderability | MIL-STD-883F, Method 2003 |
| Moisture Sensitivity Level | MSL1 @ 260°C |

Waveform Diagrams

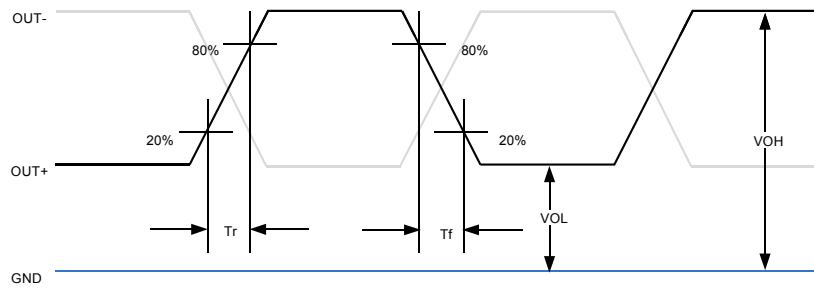


Figure 1(a). LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

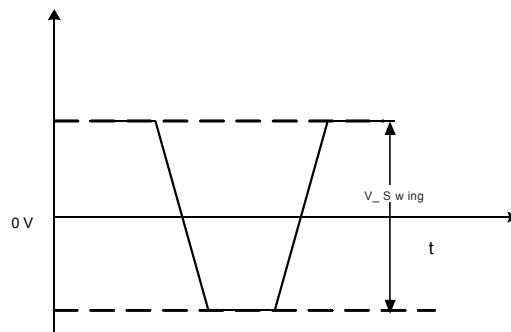


Figure 1(b). LVPECL Voltage Levels Across Differential Pair

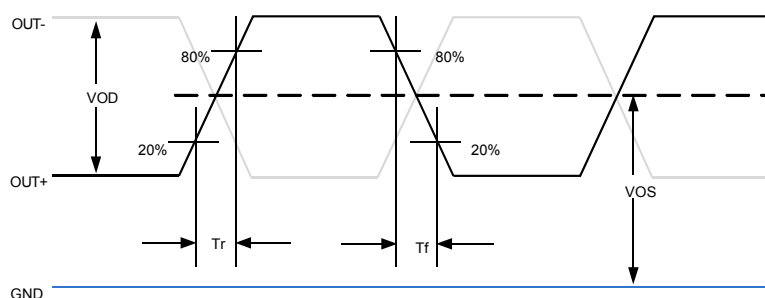


Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

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Termination Diagrams

LVPECL:

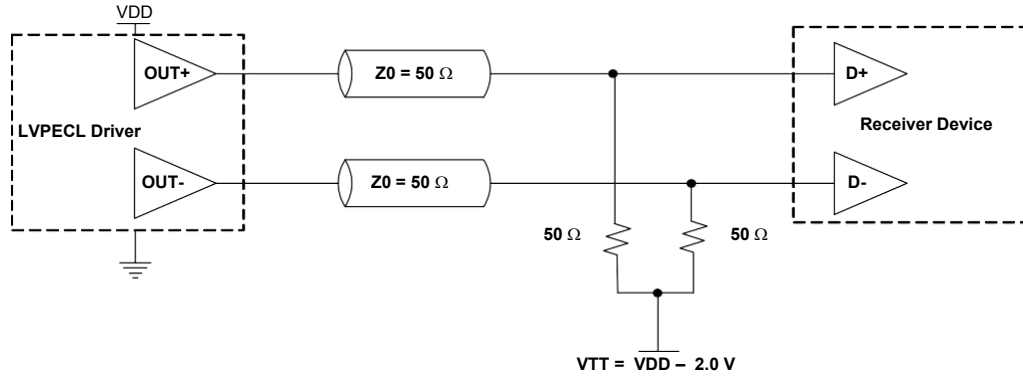


Figure 3. LVPECL Typical Termination

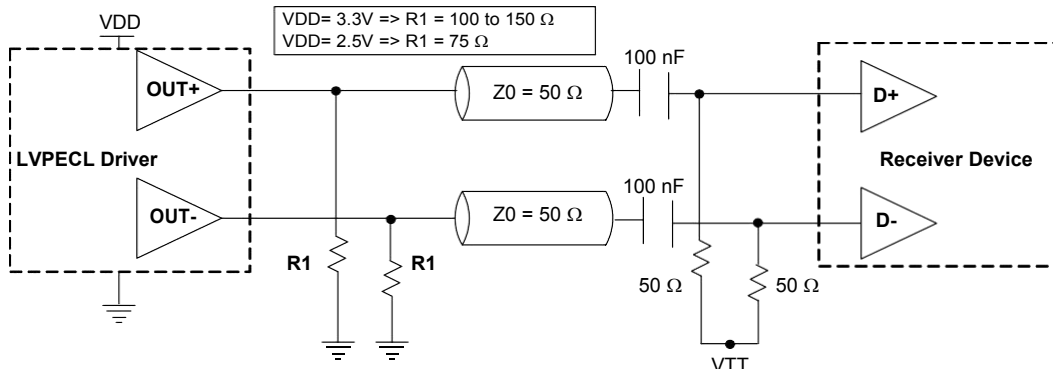


Figure 4. LVPECL AC Coupled Termination

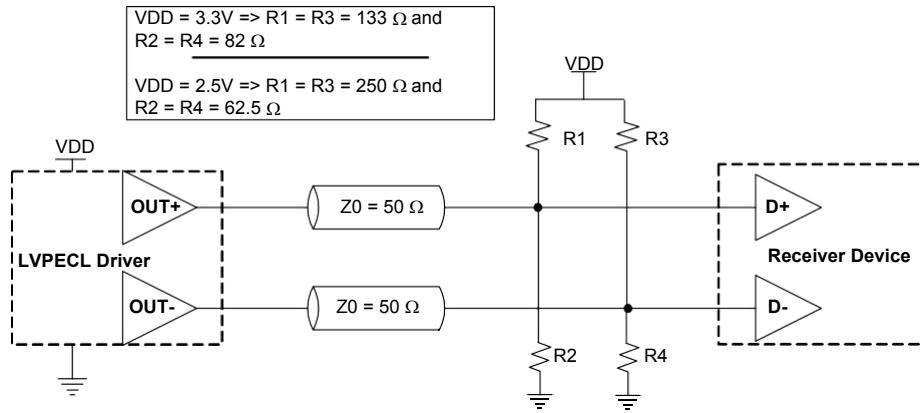


Figure 5. LVPECL with Thevenin Typical Termination

LVDS:

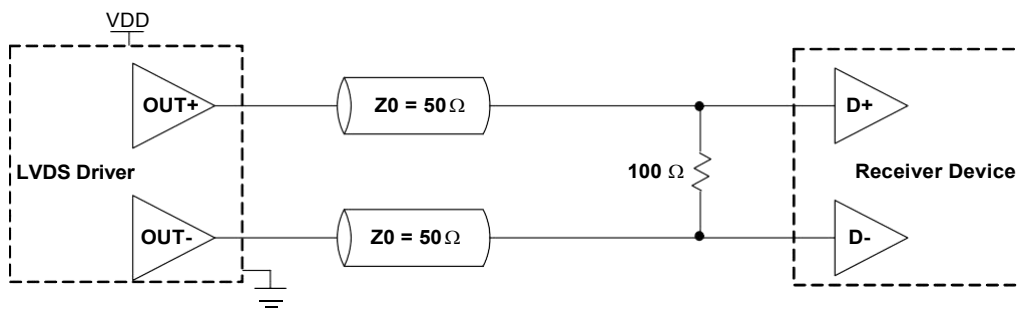


Figure 6. LVDS Single Termination (Load Terminated)