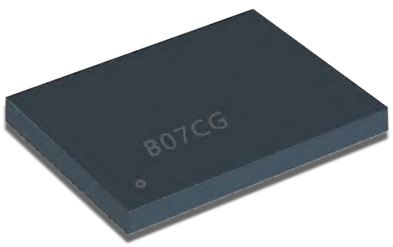
YSO8209MR



Features

- Any frequency between 80.000001 and 220 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based oscillators
- Ultra low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Frequency stability as low as ±10 PPM
- Industrial or extended commercial temperature range
- LVCMOS/LVTTL compatible output Standby or output enable modes
- Standard 4-pin packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm^2
- Outstanding silicon reliability of 2 FIT or 500 million hour MTBF
- Ultra short lead time

Applications

- SATA, SAS, Ethernet, 10-Gigabit Ethernet, SONET, PCI Express, video, Wireless
- Computing, storage, networking, telecom, industrial control

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	80.000001	–	220	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of Initial tolerance at 25 °C, and variations over operating temperature, rated power supply voltage and load
		-20	–	+20	PPM	
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	34	36	mA	No load condition, f = 100 MHz, Vdd = 2.5V, 2.8V or 3.3V
		–	30	33	mA	No load condition, f = 100 MHz, Vdd = 1.8V
OE Disable Current	I_OD	–	–	31	mA	Vdd = 2.5V, 2.8V or 3.3V, OE = GND, output is Weakly Pulled Down
		–	–	30	mA	Vdd = 1.8 V. OE = GND, output is Weakly Pulled Down
Standby Current	I_std	–	–	70	µA	Vdd = 2.5V, 2.8V or 3.3V, $\overline{ST}$ = GND, output is Weakly Pulled Down
		–	–	10	µA	Vdd = 1.8 V. $\overline{ST}$ = GND, output is Weakly Pulled Down
Duty Cycle	DC	45	–	55	%	f <= 165 MHz, all Vdds.
		40	–	60	%	f > 165 MHz, all Vdds.
Rise/Fall Time	Tr, Tf	–	1.2	2	ns	15 pF load, 10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = -6 mA, IOL = 6 mA, (Vdd = 3.3V, 2.8V, 2.5V) IOH = -3 mA, IOL = 3 mA, (Vdd = 1.8V)
Output Voltage Low	VOL	–	–	10%	Vdd	
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	–	100	250	kΩ	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2	–	–	MΩ	Pin 1, $\overline{ST}$ logic low
Startup Time	T_start	–	7	10	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 80 MHz, For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	–	–	10	ms	In standby mode, measured from the time $\overline{ST}$ pin crosses 50% threshold. Refer to Figure 5.
RMS Period Jitter	T_jitt	–	1.5	2	ps	f = 156.25 MHz, Vdd = 2.5V, 2.8V or 3.3V
		–	2	3	ps	f = 156.25 MHz, Vdd = 1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	1	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz
First year Aging	F_aging	-1.5	–	+1.5	PPM	25°C
10-year Aging		-5	–	+5	PPM	25°C

Note:

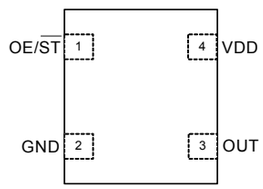
1. All electrical specifications in the above table are specified with 15 pF ±10% output load and for all Vdd(s) unless otherwise stated.
2. Contact YXC for custom drive strength to drive higher or multiple load, or SoftEdge™ option for EMI reduction.

YSO8209MR

Pin Configuration

Pin	Symbol	Functionality	
1	OE/ $\overline{ST}$	Output Enable	H or Open[3]: specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H or Open[3]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
2	GND	Power	Electrical ground
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage

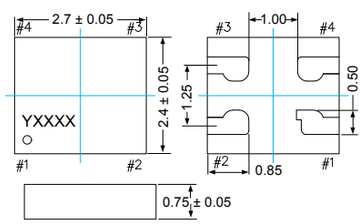
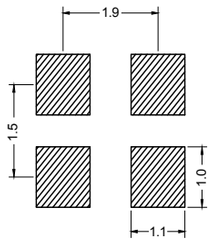
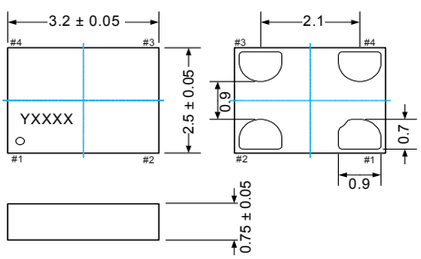
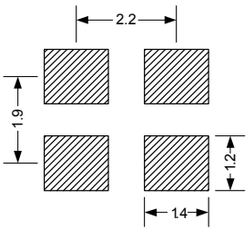
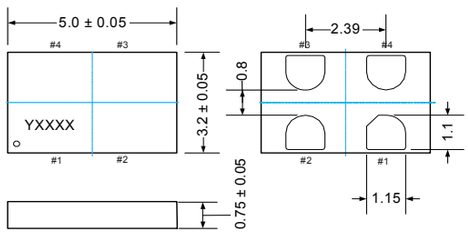
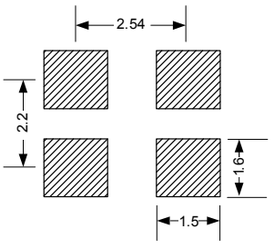
Top View



Note:

3. A pull-up resistor of <10 kΩ between OE/ $\overline{ST}$ pin and Vdd is recommended in high noise environment

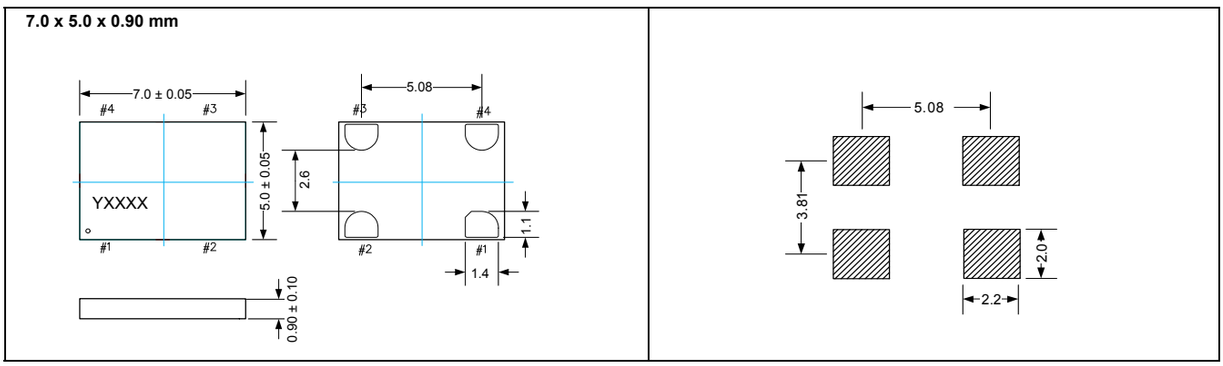
Dimensions and Patterns

Package Size – Dimensions (Unit: mm) [4]	Recommended Land Pattern (Unit: mm) [5]
2.7 x 2.4 x 0.75 mm (100% compatible with 2.5 x 2. 0 mm footprint)	
	
3.2 x 2.5 x 0.75 mm	
	
5.0 x 3.2 x 0.75 mm	
	

YSO8209MR

Dimensions and Patterns

7.0 x 5.0 x 0.90 mm



Notes:

4. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
5. A capacitor of value 0.1 µF between Vdd and GND is recommended.

PART Number Guide

Quartz Crystal Oscillator	Dimensions	Frequency (Hz)	Supply voltage (V)	Frequency Stability Overall (ppm)	Output	Pin	Material	Operating Temp. Range
O	7050	125M	E	D	H	4	M	I

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	191	263	30
5032	97	199	24
3225	109	212	27
2520	117	222	26

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Phase Noise Plot

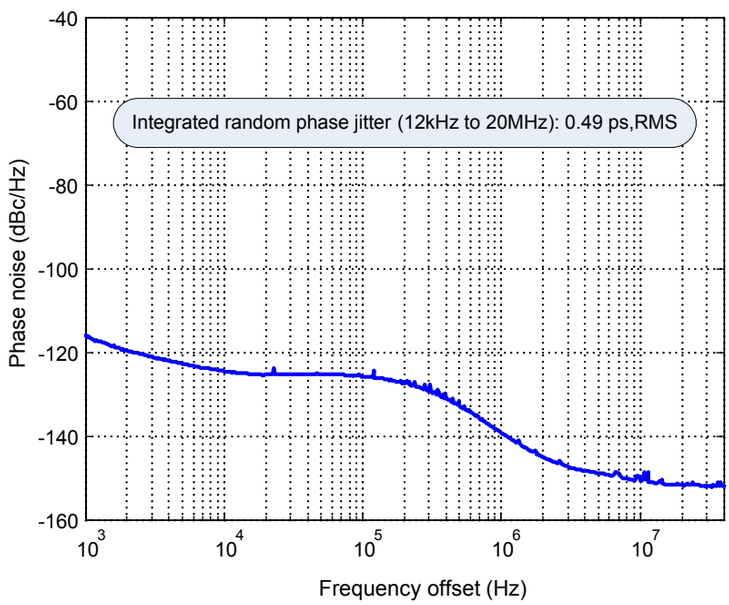


Figure 1. Phase Noise, 156.25 MHz, 3.3V, LVCMOS Output

Test Circuit and Waveform

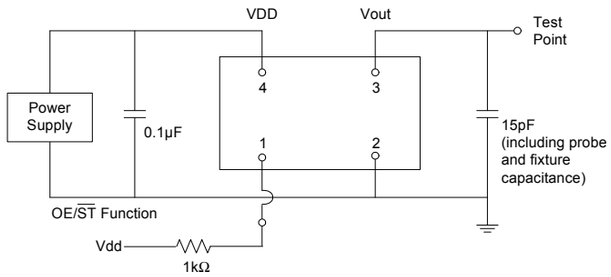


Figure 2. Test Circuit

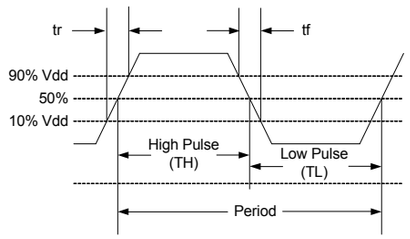


Figure 3. Waveform

Notes:

6.Duty Cycle is computed as Duty Cycle = TH/Period.

7. YSO8209MR supports the configurable duty cycle feature.

Timing Diagram

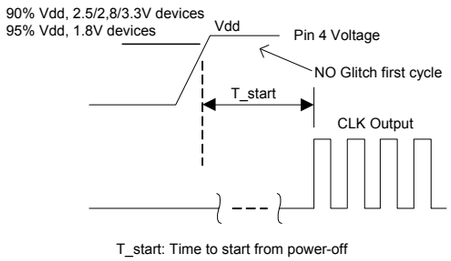


Figure 4. Startup Timing (OE/$\overline{ST}$ Mode)

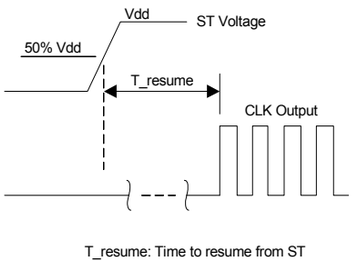


Figure 5. Standby Resume Timing ($\overline{ST}$ Mode Only)

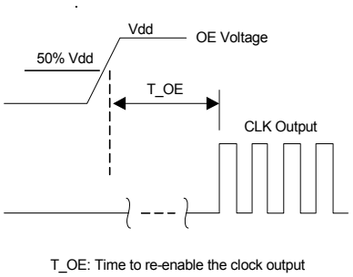


Figure 6. OE Enable Timing (OE Mode Only)

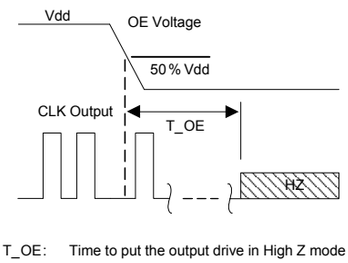


Figure 7. OE Disable Timing (OE Mode Only)

Notes:

8. YSO8209MR supports NO RUNT pulses and No glitches during startup or resume.

9. YSO8209MR supports gated output which is accurate within rated frequency stability from the first cycle.

Performance Plots

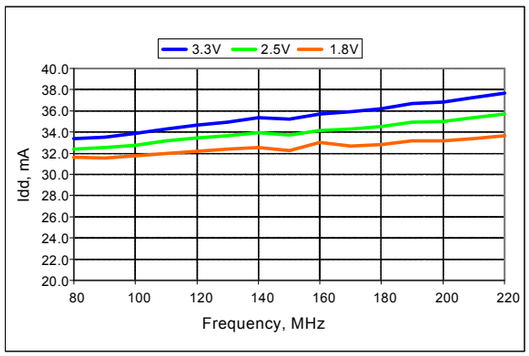


Figure 8. Idd vs Frequency

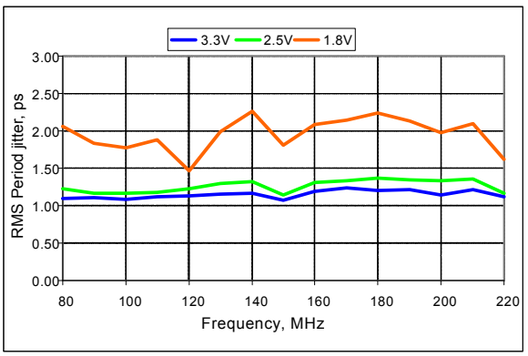


Figure 9. RMS Period Jitter vs Frequency

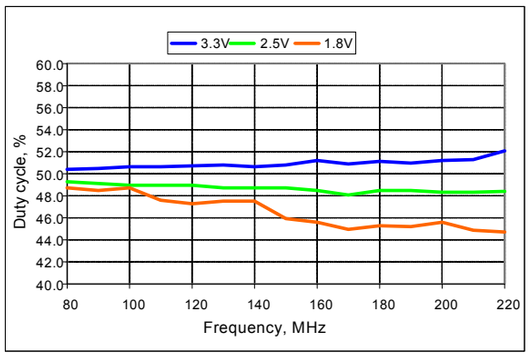


Figure 10. Duty Cycle vs Frequency

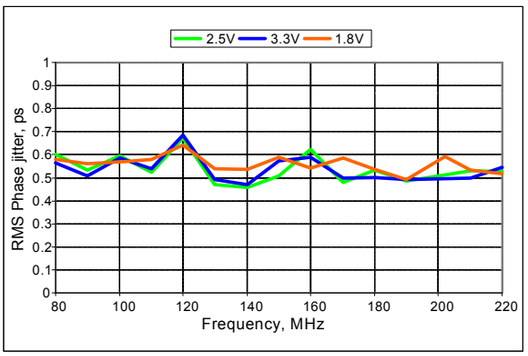


Figure 11. RMS Phase Jitter vs Frequency

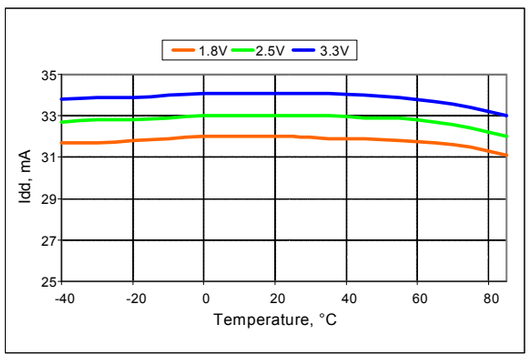


Figure 12. Idd vs Temperature, 100 MHz Output

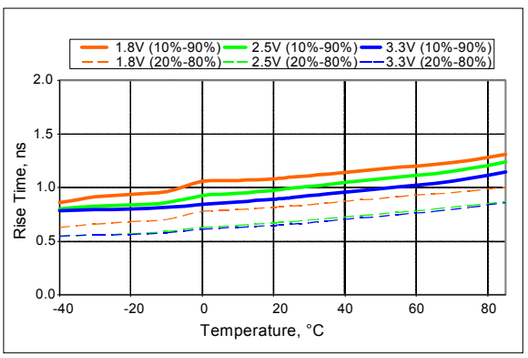


Figure 13. Rise Time vs Temperature, 100 MHz Output

Note:

10. All plots are measured with 15pF load at room temperature, unless otherwise stated.